What is claimed is:

1. A method for forming a wafer, comprising:

forming a predetermined contour in one of a semiconductor membrane and a substrate wafer; and

bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane.

2. The method of claim 1, wherein the predetermined contour is straightened when the semiconductor membrane is bonded to the substrate wafer.

3. The method of claim 1, wherein the semiconductor membrane is bonded to the substrate wafer before the predetermined contour is straightened.

4. The method of claim 3, wherein bonding the semiconductor membrane to the substrate wafer includes performing a bond cut process to form the semiconductor membrane and to bond the membrane to the substrate wafer.

5. The method of claim 1, wherein upon bonding, the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate.

6. The method of claim 1, wherein:

forming a predetermined contour in one of a semiconductor membrane and a substrate wafer includes applying a pressure to flex the substrate wafer to have a predetermined strain; and

bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane includes:

bonding a periphery of the membrane to a periphery of the substrate wafer; and

removing the pressure to relax the substrate wafer and transfer strain from the substrate wafer to the semiconductor membrane.

7. The method of claim 6, wherein applying a pressure to flex the substrate wafer to have a predetermined strain includes applying a pressure to a substrate wafer having a thickness sufficiently small such that the substrate wafer is flexible.

8. The method of clam 6, wherein applying a pressure to flex the substrate wafer to have a predetermined strain includes applying a pressure to a substrate wafer having voids such that the substrate wafer is flexible.

9. The method of claim 1, wherein:

forming a predetermined contour in one of a semiconductor membrane and a substrate wafer includes polishing a surface of a sacrificial wafer; and

bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane includes performing a bond cut process to form and bond the semiconductor membrane to the substrate wafer such that the bonding flattens and strains the semiconductor membrane.

10. The method of claim 1, wherein:

forming a predetermined contour in one of a semiconductor membrane and a substrate wafer includes forming a contoured surface in a crystalline wafer; and

bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane includes:

bonding the contoured surface to the wafer substrate; and

polishing the crystalline wafer to thin the wafer and control strain in the crystalline wafer.

11. The method of claim 1, wherein the semiconductor membrane includes silicon.

12. The method of claim 1, wherein the substrate wafer is selected from the group comprising: glass, quartz, silicon oxycarbide glass, aluminum oxycarbide glass, and silicon.

13. The method of claim 1, wherein the semiconductor membrane includes an ultra-thin semiconductor layer.

14. The method of claim 1, wherein the semiconductor membrane is between approximately 300 Å to 1000 Å.

15. The method of claim 1, further comprising forming voids in the substrate wafer to provide the substrate wafer with a desired flexibility.

16. A method for forming a wafer, comprising:

flexing a substrate wafer into a flexed position;

bonding a portion of the substrate wafer to a semiconductor layer when the substrate wafer is in the flexed position; and

relaxing the substrate wafer to induce a predetermined strain in the semiconductor layer.

17. The method of claim 16, wherein the semiconductor layer is an ultra-thin silicon membrane.

18. The method of claim 16, wherein the substrate wafer is selected from the group comprising: glass, quartz, silicon oxycarbide glass, aluminum oxycarbide glass, and silicon.

19. The method of claim 16, wherein the predetermined strain is within a range between approximately 0.75% and approximately 1.5%.

20. The method of claim 16, wherein the predetermined strain is within a range between approximately 1.0% and approximately 1.2%.

21. The method of claim 16, further comprising bonding a composite of the silicon membrane and the substrate wafer to a carrier wafer.

22. A method for forming a wafer, comprising:

flexing a central region of a substrate wafer into a flexed position;

bonding a peripheral region of the substrate wafer to a peripheral region of a silicon membrane when the substrate wafer is in the flexed position;

relaxing the substrate wafer to induce a predetermined strain in the silicon membrane.

23. The method of claim 22, wherein relaxing the substrate wafer to induce a predetermined strain in the silicon membrane includes inducing a strain in the silicon membrane greater than 0.5%.

24. The method of claim 22, wherein relaxing the substrate wafer to induce a predetermined strain in the silicon membrane includes inducing a strain in the silicon membrane within a range between approximately 0.75% to approximately 1.5%.

25. The method of claim 22, wherein relaxing the substrate wafer to induce a predetermined strain in the silicon membrane includes inducing a strain in the silicon membrane between approximately 1% to approximately 1.2%.

26. The method of claim 22, further comprising bonding a composite of the silicon membrane and the substrate wafer to a carrier wafer.

27. The method of claim 22, wherein the semiconductor layer is an ultra-thin silicon membrane.

28. A method for forming a wafer, comprising:

flexing a central region of a substrate wafer into a flexed position;

performing a bond cut process to form a silicon membrane from a crystalline sacrificial wafer and bond a peripheral region of the substrate wafer to a peripheral region of a silicon membrane when the substrate wafer is in the flexed position; and

relaxing the substrate wafer to induce a predetermined strain in the silicon membrane.

29. The method of claim 28, wherein performing a bond cut process includes:

defining the silicon membrane in a surface layer of a sacrificial crystalline silicon wafer;

bonding the surface layer of the sacrificial wafer to the peripheral region of the substrate wafer;

heat-treating the sacrificial wafer and the substrate wafer; and

separating the sacrificial wafer from the membrane such that the silicon membrane remains strongly bonded to the substrate wafer.

30. The method of claim 28, wherein:

defining a crystalline silicon membrane in a surface layer of a sacrificial crystalline semiconductor wafer includes implanting helium ions into the sacrificial wafer to form cavities along a cleavage plane; and

heat-treating the sacrificial wafer and the substrate wafer combines cavities along the cleavage plane such that the sacrificial wafer is separated from the silicon membrane along the cleavage plane.

31. A method for forming a wafer, comprising:

forming voids in a substrate wafer to provide the substrate wafer with a desired flexibility;

flexing the substrate wafer into a flexed position;

bonding a portion of the substrate wafer to a semiconductor membrane when the substrate wafer is in the flexed position; and

relaxing the substrate wafer to induce a predetermined strain in the semiconductor membrane.

32. The method of claim 31, wherein the semiconductor membrane includes a silicon membrane having a thickness between approximately 300 Å and

approximately 1000 Å, and the predetermined strain is within a range between approximately 0.75% and approximately 1.5%.

33. The method of claim 31, wherein forming voids in a substrate wafer includes forming a predetermined arrangement of voids using a surface transformation process.

34. The method of claim 31, wherein bonding a portion of the substrate wafer to a semiconductor membrane includes performing a bond cut process.

35. The method of claim 31, wherein forming voids in a substrate wafer includes forming holes in a substrate wafer having a well-defined melting temperature, and annealing the substrate wafer at a temperature that is close to and below the well-defined melting temperature.

36. The method of claim 31, wherein forming voids in a substrate wafer includes forming spherical voids using a surface transformation process, each of the spherical voids being a predetermined size and being positioned at a predetermined location.

37. The method of claim 31, wherein forming voids in a substrate wafer includes forming pipe-shaped voids using a surface transformation process, each of the pipe-shaped voids being a predetermined size and being positioned at a predetermined location.

38. The method of claim 31, wherein forming voids in a substrate wafer includes forming plate-shaped voids using a surface transformation process, each of the plate-shaped voids being a predetermined size and being positioned at a predetermined location.

39. A method for forming a wafer, comprising:

forming a convex contour in a surface of a sacrificial crystalline wafer; and

performing a bond cut process to form an ultra-thin semiconductor membrane and bond the ultra-thin semiconductor membrane to a substrate wafer, wherein the ultra-thin semiconductor membrane is flattened and strained when bonded to the substrate wafer.

40. The method of claim 39, wherein the ultra-thin semiconductor membrane includes a silicon membrane.

41. The method of claim 39, wherein performing a bond cut process includes:

defining the semiconductor membrane in a surface layer of a sacrificial crystalline silicon wafer;

bonding the surface layer of the sacrificial wafer to the peripheral region of the substrate wafer;

heat-treating the sacrificial wafer and the substrate wafer; and

separating the sacrificial wafer from the semiconductor membrane such that the semiconductor membrane remains strongly bonded to the substrate wafer.

42. The method of claim 39, wherein:

defining a crystalline semiconductor membrane in a surface layer of a sacrificial crystalline semiconductor wafer includes implanting helium ions into the sacrificial wafer to form cavities along a cleavage plane; and

heat-treating the sacrificial wafer and the substrate wafer combines cavities along the cleavage plane such that the sacrificial wafer is separated from the semiconductor membrane along the cleavage plane.

43. A method for forming a wafer, comprising:

forming a concave surface in a crystalline wafer;

bonding the concave surface of the crystalline wafer to a substrate wafer to induce a strain in the crystalline wafer; and

polishing the bonded crystalline wafer to thin the crystalline wafer and control the induced strain.

44. A method of forming a transistor, comprising:

straining a semiconductor layer to form a strained semiconductor layer, including:

forming a predetermined contour in one of a semiconductor layer and a substrate wafer; and

bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer;

forming a gate separated from the strained semiconductor layer by a gate insulator; and

forming first and second diffusion regions separated by a channel region, the strained semiconductor layer including the first and second diffusion region and the channel region.

45. The method of claim 44, wherein the semiconductor layer is wafer-sized.

46. The method of claim 44, wherein:

forming a predetermined contour in one of a semiconductor layer and a substrate wafer includes applying a pressure to flex the substrate wafer to have a predetermined strain; and

bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer includes:

bonding a periphery of the semiconductor layer to a periphery of the substrate wafer; and

removing the pressure to relax the substrate wafer and transfer strain from the substrate wafer to the semiconductor layer.

47. A method of forming a transistor, comprising:

forming a strained silicon membrane on a substrate wafer, including:

flexing a central region of the substrate wafer into a flexed position;

bonding a peripheral region of the substrate wafer to a peripheral region of the silicon membrane when the substrate wafer is in the flexed position; and

relaxing the substrate wafer to induce a predetermined strain in the silicon membrane;

forming a gate separated from the strained silicon membrane by a gate insulator; and

forming first and second diffusion regions separated by a channel region, the strained silicon membrane including the first and second diffusion region and the channel region.

48. The method of claim 47, wherein the strained silicon membrane is wafer-sized.

49. The method of claim 47, wherein the substrate wafer has a thickness sufficiently small such that the substrate wafer has a desired flexibility.

50. The method of claim 49, further comprising bonding a composite of the substrate wafer and the silicon membrane to a carrier substrate.

51. The method of claim 47, further comprising forming voids in the substrate wafer such that the substrate wafer has a desired flexibility.

52. A method of forming a memory array, comprising:

forming a substrate with a strained silicon layer, including:

flexing a central region of a substrate wafer into a flexed position;

bonding a peripheral region of the substrate wafer to a peripheral region of the silicon layer when the substrate wafer is in the flexed position; and

relaxing the substrate wafer to induce a predetermined strain in the silicon layer;

forming a plurality of memory cells using the strained silicon layer, including arranging the memory cells in rows and columns and forming at least one transistor for each of the plurality of memory cells, wherein forming at least one transistor includes:

forming a gate separated from the strained silicon layer by a gate insulator; and

forming first and second diffusion regions separated by a channel region, the strained silicon layer including the first and second diffusion region and the channel region;

forming a plurality of word lines, including connecting each word line to a row of memory cells; and

forming a plurality of bit lines, including connecting each bit line to a column of memory cells.

53. A method for forming an electronic system, comprising:

forming a strained semiconductor layer, including:

forming a predetermined contour in one of a semiconductor layer and a substrate wafer; and

bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer;

forming a processor and forming a memory device in communication with the processor, wherein forming a processor and forming a memory device includes forming at least one transistor with a channel region formed by the strained semiconductor layer.

54. A wafer structure, comprising:

a substrate wafer having a predetermined Youngs modulus of elasticity and a predetermined thickness to provide the substrate wafer with a desired flexibility to bow from a relaxed position into a flexed position under a predetermined force; and

a wafer-sized strained semiconductor layer bonded to the substrate wafer, the strained semiconductor layer having a strain induced by relaxing the substrate wafer from the flexed position.

55. The wafer structure of claim 54, further comprising a carrier substrate, wherein the substrate wafer is bonded to the carrier substrate.

56. The wafer structure of claim 54, wherein the semiconductor layer has a strain greater than 0.5%.

57. The wafer structure of claim 54, wherein the semiconductor layer has a strain within a range between approximately 0.75% and approximately 1.5%.

58. A wafer structure, comprising:

a substrate wafer having a peripheral region; and

a strained semiconductor layer having a peripheral region bonded to the peripheral region of the substrate wafer and a central region within the peripheral region, wherein the central region has a strain induced by relaxing the substrate wafer from a flexed position to a relaxed position.

59. The wafer structure of claim 58, wherein the strained semiconductor layer includes silicon.

60. The wafer structure of claim 58, wherein the strained semiconductor layer includes an ultra-thin semiconductor layer.

61. The wafer structure of claim 58, wherein the strained semiconductor layer includes a semiconductor layer having a thickness between approximately 300 Å and approximately 1000 Å.

62. The wafer structure of claim 58, wherein the strained semiconductor layer includes a strained silicon layer having a strain within a range between approximately 0.75% to approximately 1.5%.

63. The wafer structure of claim 58, wherein the substrate wafer is selected from the group comprising: glass, quartz, silicon oxycarbide glass, aluminum oxycarbide glass, and silicon.

64. The wafer structure of claim 58, wherein the substrate wafer includes voids to provide the substrate wafer with a desired flexibility.

65. The wafer structure of claim 58, wherein the substrate wafer includes a predetermined arrangement of voids formed by surface transformation to provide the substrate wafer with a desired flexibility.